FIG. 1

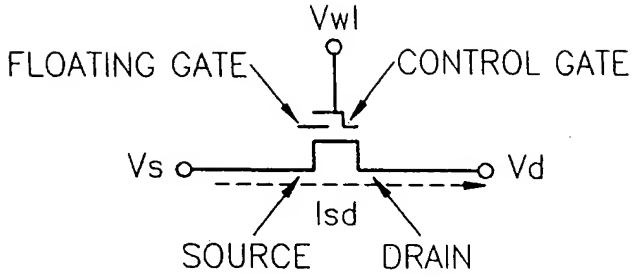

Vwl
FLOATING GATE
CONTROL GATE
Vs
Vd
Isd
SOURCE
DRAIN

FIG. 2

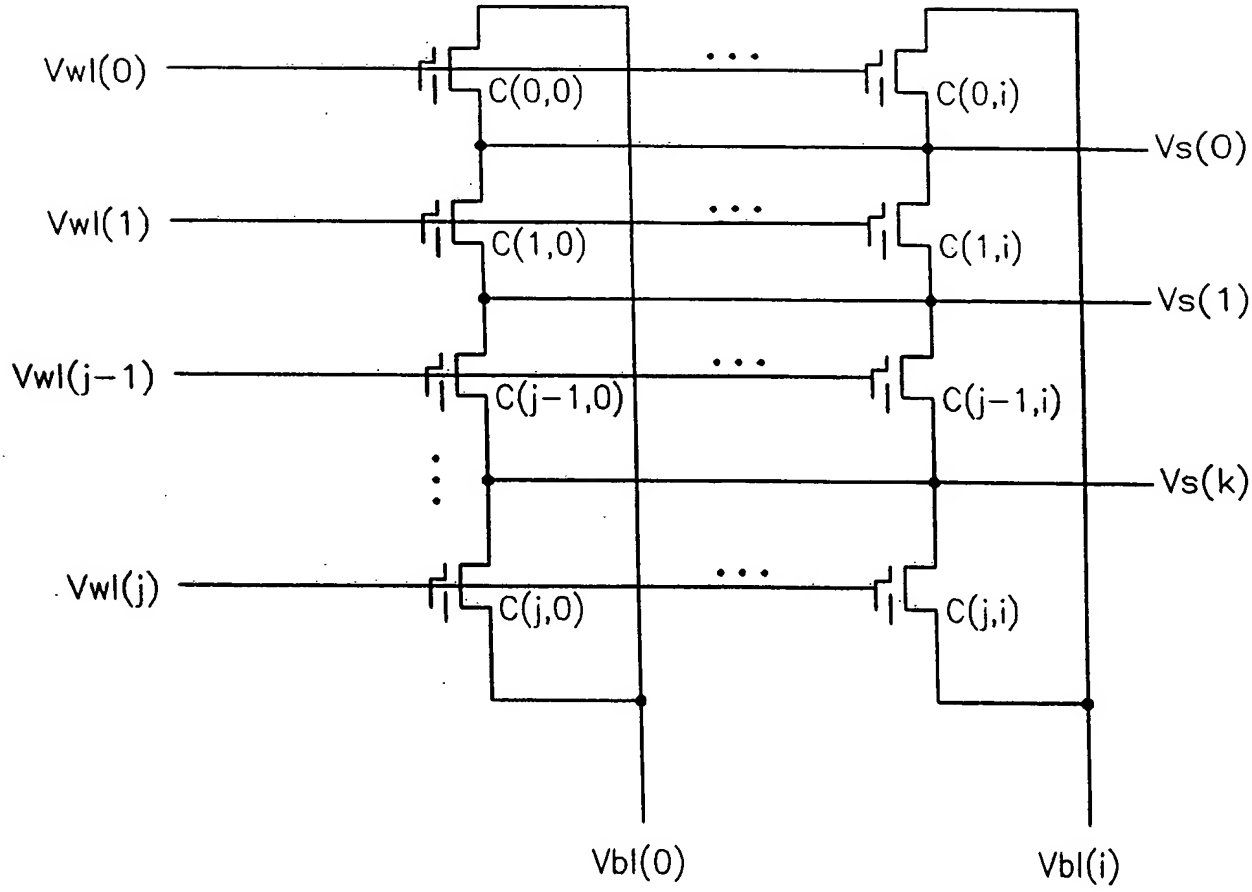

Vwl(0)
Vwl(1)
Vwl(j-1)
Vwl(j)
C(0,0)
C(0,i)
C(1,0)
C(1,i)
C(j-1,0)
C(j-1,i)
C(j,0)
C(j,i)
Vs(0)
Vs(1)
Vs(k)
Vbl(0)
Vbl(i)

FIG. 3

OPERATION	Vwl [V]	Vs [V]	Vbl [V]
READING	1.5	0	0.7
PROGRAMMING	1.4	8	0.4
ERASURE	11.0	0	0

FIG. 4 (PRIOR ART)

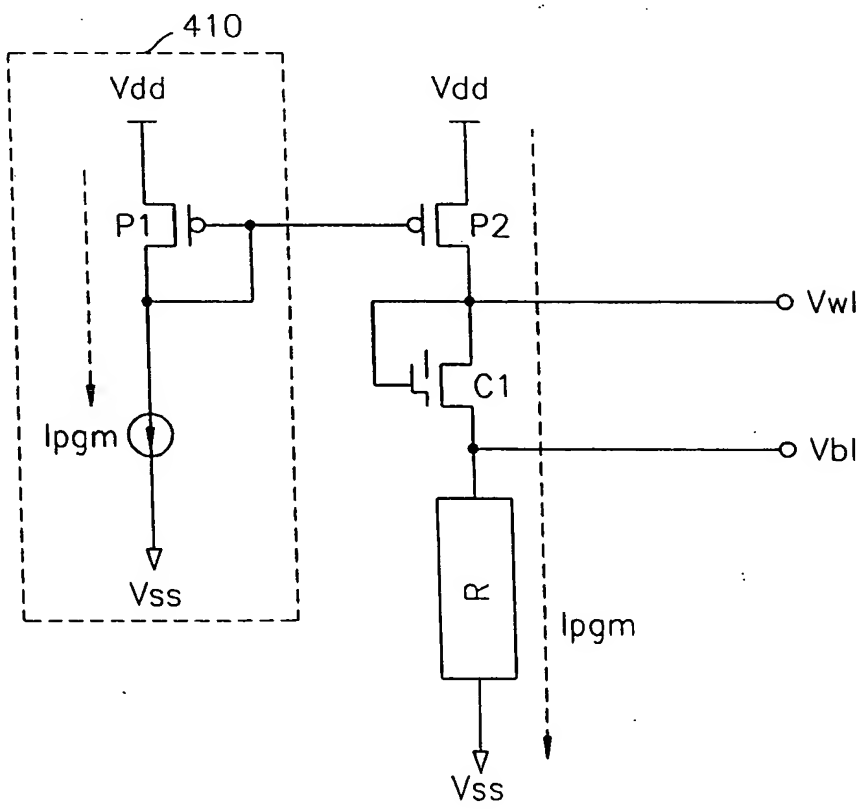


FIG. 5 (PRIOR ART)

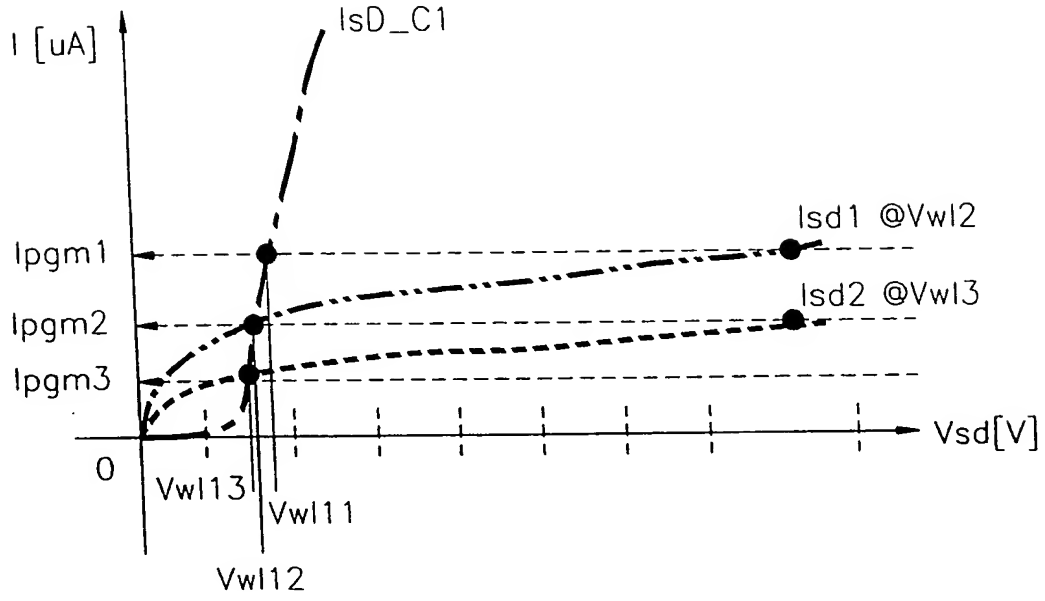


FIG. 6 (PRIOR ART)

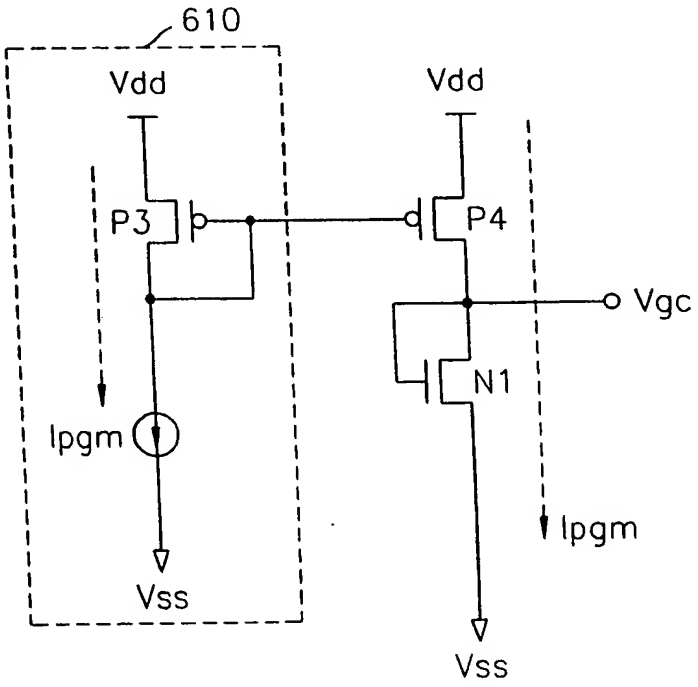


FIG. 7 (PRIOR ART)

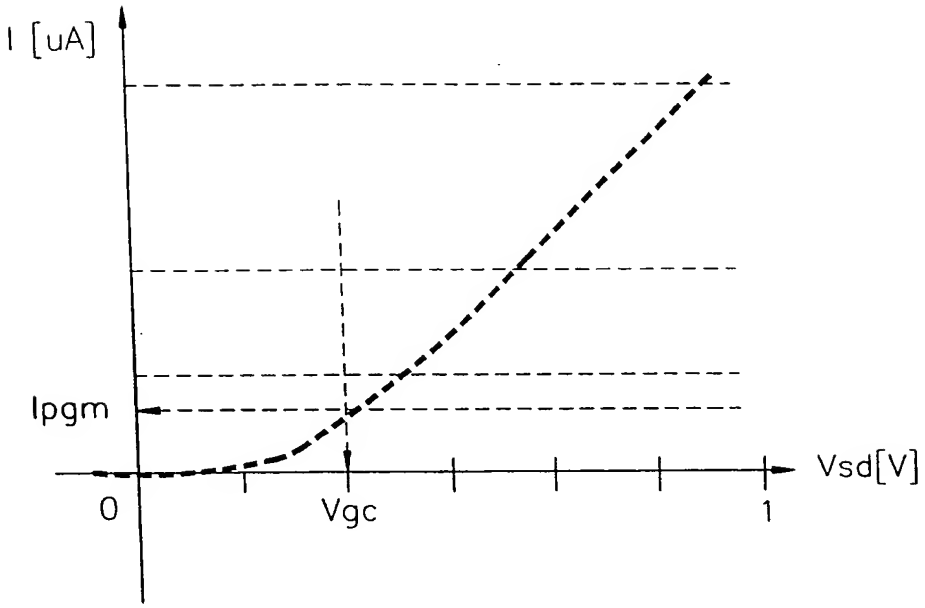


FIG. 8 (PRIOR ART)

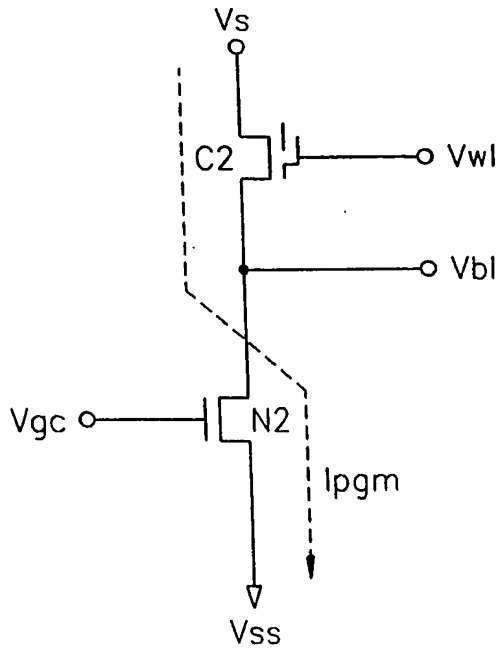


FIG. 9

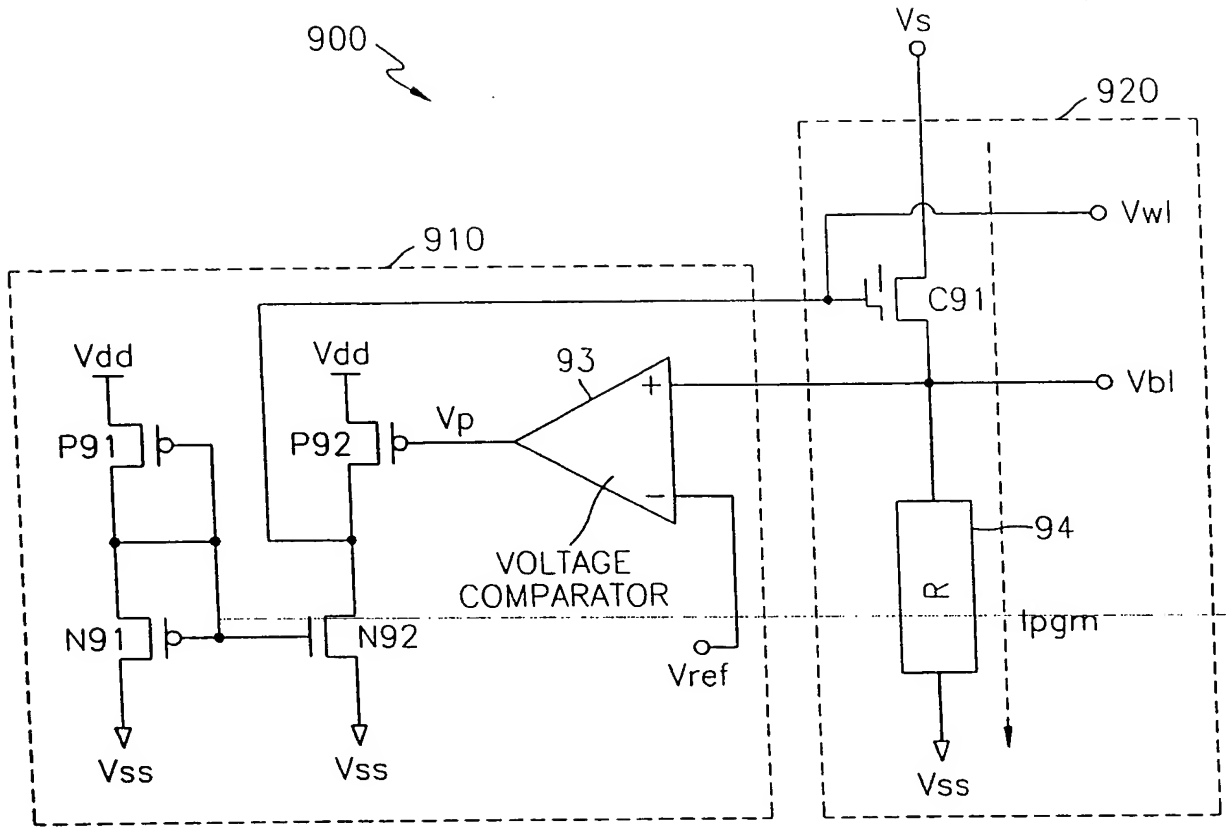

900
Vs
920
Vwl
910
C91
Vdd
Vdd
93
Vbl
P91
P92
Vp
+
−
94
VOLTAGE
COMPARATOR
N91
N92
Ipgm
Vref
Vss
Vss
Vss

FIG. 10

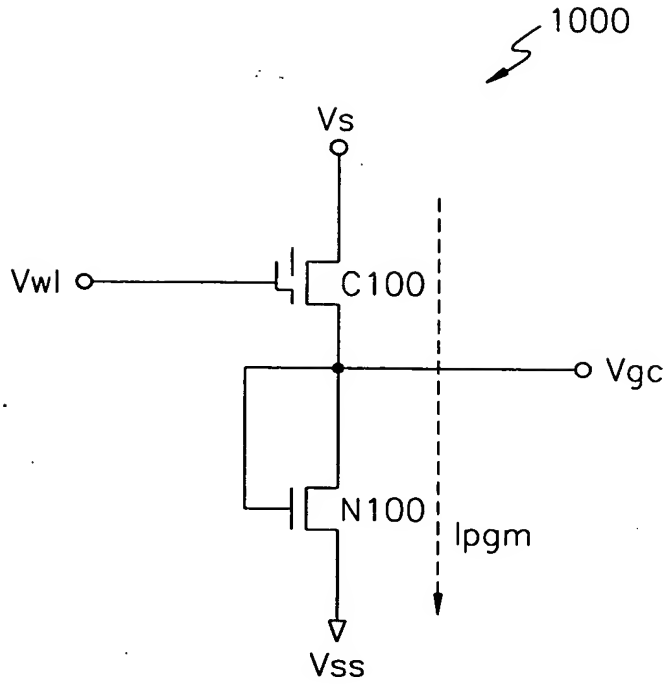
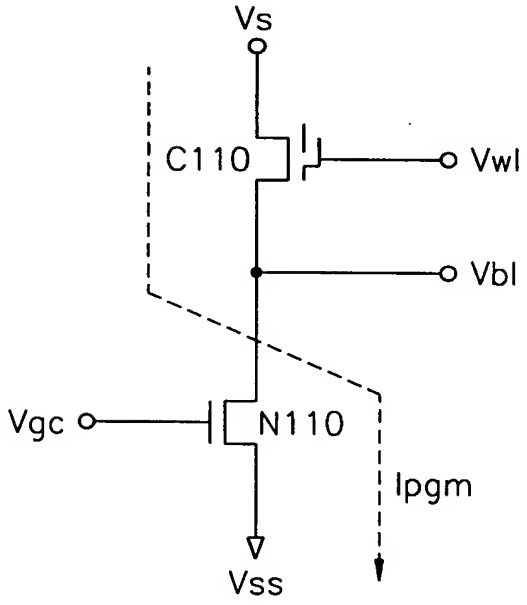

1000
Vs
Vwl
C100
Vgc
N100
Ipgm
Vss

FIG. 11


Vs
C110
Vwl
Vbl
Vgc
N110
Ipgm
Vss